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An On-Chip SiC MEMS Device with Integrated Heating, Sensing, and Microfluidic Cooling Systems

Toan Dinh, Hoang-Phuong Phan, Navid Kashaninejad, Tuan-Khoa Nguyen, Dzung Viet Dao, and Nam-Trung Nguyen*

There has been increasing interest in electronic systems with integrated microfluidic active cooling modules. However, the failure of 3C-SiC/Si interface with increasing temperature has prevented the development of 3C-SiC power electronic devices. Here, all integrated transparent heating, sensing, and cooling systems are developed on a single silicon carbide (SiC) chip for efficient thermal management. SiC nanofilms are grown on a silicon wafer, are transferred to a glass substrate, and then a micro electromechanical system process is employed to fabricate a SiC-on-glass system with integrated heaters and temperature sensors. A cooling system is fabricated with microchannel using 3D printing, molding, and plasma assisted bonding. The thermal management of the SiC-based system shows an excellent capability of heating and detecting temperature as well as effective cooling with an efficiency of from 0.24 to 0.28 and a maximum cooling rate of 0.1 K(μL min^{-1})$^{-1}$. The fabrication strategy can be utilized for large production of SiC power nanoelectronics with high efficiency of integrated thermal management systems.

1. Introduction

The development of integrated circuit and micro electromechanical system (MEMS) has been driven toward low cost, large scale production, high density, and fast operation speed.[1,2] The factors led to the increasing operation temperature of microdevices, which affect their performance and reliability.[3–5] Therefore, on-chip thermal management of microsystems has played an important role in improving their efficiency, reliability, and performance.[6,7]

Integrated thin-film resistive heater has been successfully demonstrated to precisely control the temperature of a microsystem.[8–10] However, current cooling technologies including air and water pumps have faced difficulties in integration into the power electronic systems as these systems typically require integrated temperature sensors for cooling feedback to improve the efficiency of the cooling system.[11,12] In addition, integrating all these functions in a microsystem has been a great challenge. Therefore, there is a need for the development of an on-chip system with integrated heating, cooling, and sensing.

Silicon carbide (SiC) has been proven to be an unprecedented material for high power electronics and integrated microsystems, owing to its excellent thermal properties and compatibility with mature conventional micro-/nanomachining technologies.[13–15] High-quality SiC nanofilms with their high electrical conductivity have been already reported.[16] Consequently, numerous sensing effects in SiC have been investigated including its high thermoresistive effect,[17–22] showing great potential of using SiC material for both heating and sensing. However, the leakage current from SiC to the Si substrate at elevated temperature has prevented the integration of heating, sensing, and cooling systems into SiC MEMS and power electronics.[23] This current challenge for the development of the SiC/Si power electronics is due to the failure of the 3C-SiC/Si interfaces (i.e., heterojunctions) at elevated temperatures. Our successful demonstration of transferring high-quality SiC nanofilm onto a glass substrate would enable the development of fully integrated heating, sensing, and cooling on a single chip.[24]

In this work, we report on the development of these SiC devices. We used single crystalline SiC nanofilms grown on SiC and subsequently transferred them to glass substrates to fabricate both hot film heating element and thermoresistive temperature sensors. We employed MEMS processes including photolithography and reactive ion etching to form these heating and sensing components. 3D printing, molding, and plasma-assisted bonding were used to fabricate the cooling channels. In addition, the cooling system was characterized with single-phase water flow under different input heating powers and water flow rates. Our fabrication strategy can completely eliminate the disadvantages of the 3C-SiC/Si interface, enabling the development of integrated temperature-controllable 3C-SiC power electronics.

Dr. T. Dinh, Dr. H.-P. Phan, Dr. N. Kashaninejad, T.-K. Nguyen, Prof. D. V. Dao, Prof. N.-T. Nguyen
Queensland Micro- and Nanotechnology Centre
Griffith University
Brisbane, Queensland 4111, Australia
E-mail: toan.dinh@griffithuni.edu.au

Prof. D. V. Dao
School of Engineering and Built Environment
Griffith University
Gold Coast, Queensland 4222, Australia

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/admi.201800764.

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2. Material, Fabrication, and Methods

2.1. SiC Material

SiC nanofilms with a thickness of 600 nm were grown on p-type lightly doped (10^{14} cm^{-3}) Si(100) wafers with a diameter of 150 mm and a thickness of 625 µm, using a Low Pressure Chemical Vapor Deposition approach at 1250 °C. In the growth process, silane SiH_4 and propene C_3H_6 were utilized as the precursor gases to form the SiC film, while ammonia NH_3 was employed to in situ dope the material with n-type impurity at a level of 10^{19} cm^{-3}. The thickness of the film was confirmed using a Nanospec AFT 210 (NanometricTM). Single crystalline 3C-SiC was characterized using X-ray diffraction, transmission electron microscopy, and selected area electron diffraction.[25,26] The characterization results are shown in the Supporting Information (Figure S1). The interface between SiC and Si (i.e., SiC/Si heterojunction) was investigated, indicating the presence of stacking faults and boundaries. This results in a significant current flow to the Si substrate at elevated temperatures (Figure S2, Supporting Information). **Figure 1**a shows the electrical failure of the SiC/Si interface with increasing temperature (e.g., above 50 °C), indicating the unsuitability for power electronics where the working temperature is typically above 100 °C. The details on current measurement are shown in the Supporting Information (Figure S2). Figure 1b,c shows the mechanism for the failure of the SiC/Si interface. The band offsets of 0.45 and 1.7 eV for the conduction band and the valence band, respectively, between 3C-SiC and Si could not impede the motion of carriers through the heterojunction.[27–30] This is attributed to the fact that the stacking faults and boundaries exist at the interface (Figure S1c, Supporting Information), creating the potential barriers (Figure 1b,c). The lattice mismatch between Si and SiC contributes to these boundaries and stacking faults. When the temperature increases, the carriers are generated in the Si substrate, and the thermal emission of the electrons over the energy barrier (0.45 eV) results in the electrical flow to the silicon substrate.[27,28] The transporting of holes in the valence band is attributed to the tunneling mechanism through the barrier (1.7 eV),[29,30] as shown in the Supporting Information (Figure S3). In the next section, we present our fabrication strategy to completely eliminate the negative impact of the interface, as well as integrate heating, sensing, and cooling system into a single chip. Our fabrication concept is based on the replacement of Si with SiO_2 to the source of the generated carriers, as well as to create a sufficient barrier (i.e., from SiO_2) to prevent the current flow to the substrate (**Figure 2**). Figure 2a shows the n-3C-SiC/Si structure with its energy band gap, and Figure 2b shows the platform of 3C-SiC/SiO_2 with

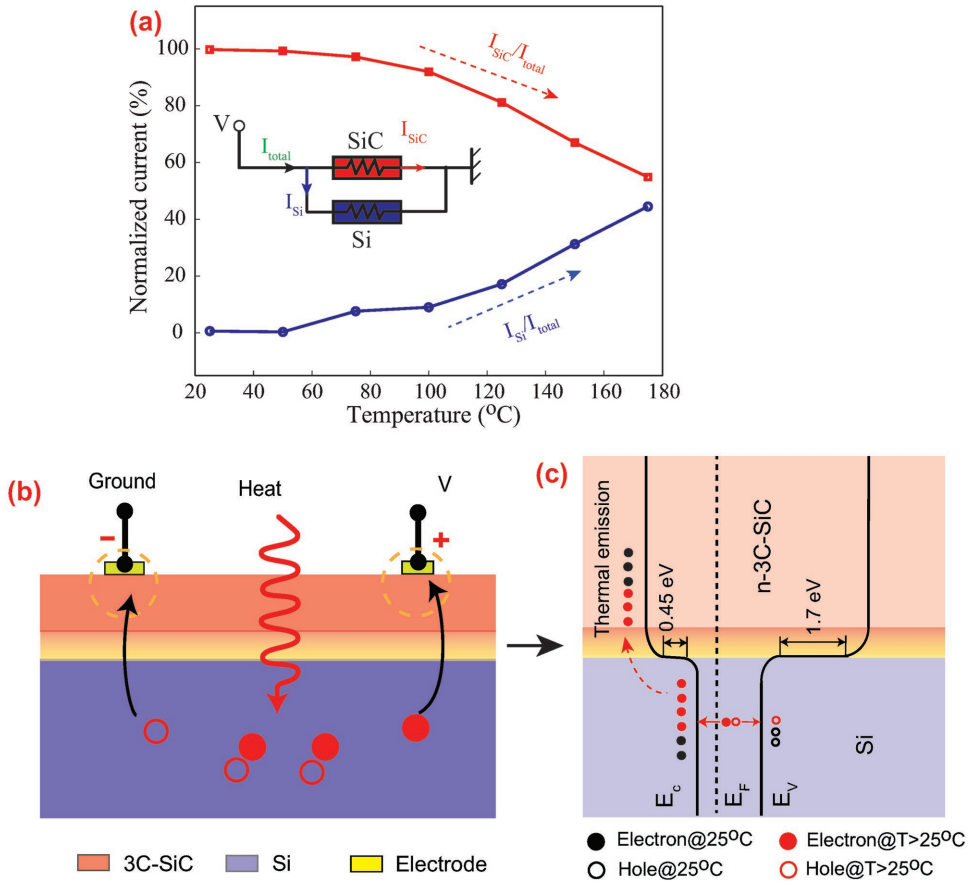

Figure 1. Temperature effect on the SiC/Si interface. a) Electrical current flow in the SiC/Si platform; b) schematic sketch of SiC/Si structure showing the generation of carriers with increasing temperature; c) transport mechanism of n-3C-SiC/Si.

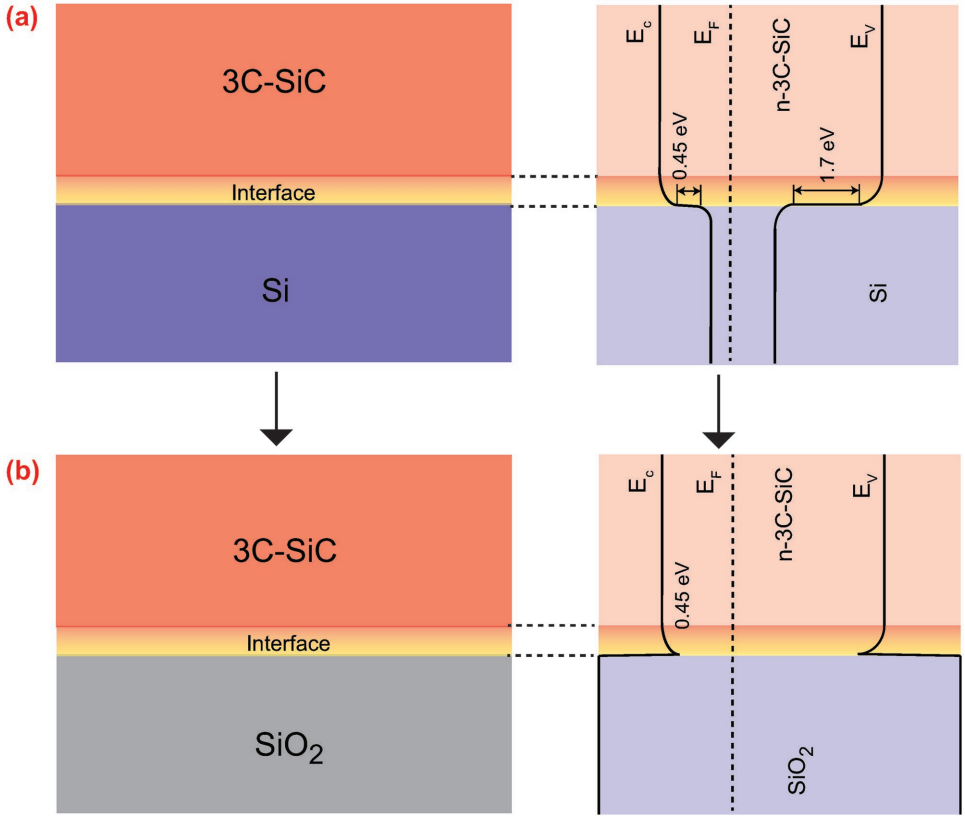

Figure 2. Fabrication strategy to eliminate the negative impact of the SiC/Si interface. a) Single crystalline n-type 3C-SiC grown on Si with its corresponding band energy structure; b) power electronic platform with 3C-SiC on glass with the corresponding band energy structure.

a very large energy band gap of SiO_2. Similarly, the p-3C-SiC on Si and SiO_2 platforms with the corresponding energy band diagrams are shown in the Supporting Information (Figure S4).

To confirm the smoothness of the SiC surface for the bonding process, we used Atomic Force Microscopy techniques to characterize the SiC film. The results indicate a roughness of less than 20 nm (not shown here) that is suitable for the subsequent bonding process. We then bonded the SiC film to a glass wafer (Boronfloat) with a thickness of 500 µm using a pressure of 137 kPa and a bias voltage of 1000 V. We confirmed the strength of the bond before a wet etching process was performed using a potassium hydroxide solution (KOH) at 80 °C to remove the 625 µm thick Si layer. **Figure 3**a shows the as-fabricated SiC on glass platform, indicating its excellent transparency. The transparent heaters employing the SiC/glass platform are potential for a wide range of applications including liquid crystal displays, window defrosters, and avionics.[31,32] Figure 3b illustrates the Raman spectrum of SiC/glass with a peak at 793.9 cm^{-1} corresponding to the TO mode of 3C-SiC material. The conductivity of the SiC film on glass was estimated to be 2.5×10^3 S m^{-1}.

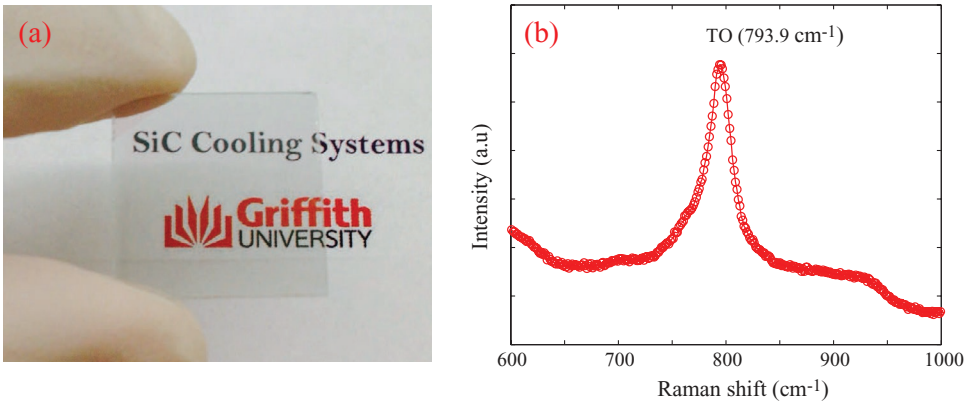

Figure 3. Single crystalline SiC on glass. a) Optical image of the SiC on glass platform showing its excellent transparency. b) Raman spectrum of SiC on glass. The peak at 793.9 cm^{-1} corresponds to the TO mode of 3C-SiC material.

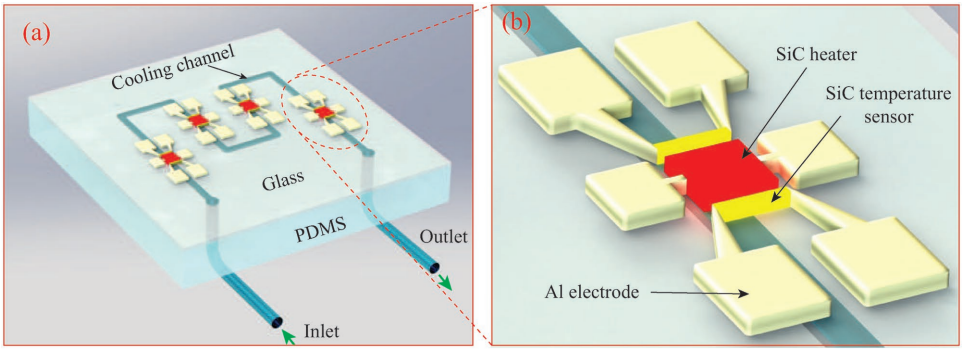

Figure 4. SiC power electronic system. a) 3D drawing of an integrated cooling device with arrays of SiC/glass heating and sensing units and a PDMS cooling channel. b) A zoom-in 3D image of a SiC heater and two surrounding SiC temperature sensors.

2.2. Design and Fabrication of SiC On-Chip System

The SiC cooling test device consists of an array of multiple heating/sensing SiC units on top of the glass substrate. A 3D-printed cooling channel is bonded on the back of the chip (**Figure 4**a). The cooling channel has a rectangular cross section of 500 μm × 200 μm and the heating/cooling unit was designed with a center-to-center spacing of 500 μm. A single heating element is a square (300 μm × 300 μm) SiC nanofilm heater, and two sensing elements (300 μm × 100 μm) are arranged on both sides of the heater with a distance of 10 μm (Figure 4b). The temperature of the device is detected via the two SiC temperature sensors. When the cooling system is ON, the water flow decreases the chip temperature, leading to a resistance change of the SiC temperature sensors. By detecting the resistance change, heating and cooling processes can be characterized.

Figure 5 shows the fabrication process for the integrated heaters and temperature sensors. The first step was the growth of the SiC nanofilm on a Si substrate (Figure 5, step 1). The SiC nanofilm was then bonded on a glass substrate (Figure 5, step 2). In the next step, Si substrate was removed to form a SiC on glass wafer (Figure 5, step 3). Then, a 1.2 μm thick positive photoresist was coated on the wafer using a spin coater at a rotational speed of 4000 rpm (Figure 5, step 4). This photoresist was then soft baked at 105 °C for 90 s and patterned as an array of heaters and temperature sensors (Figure 5, step 5) using UV light and photoresist developer. To prepare for the SiC etching process, the as-patterned photoresist is hard baked in 3 min at 120 °C. In the next step, we performed Inductively Coupled Plasma etching to pattern the SiC heaters and temperature sensors (Figure 5, step 6). In the etching process, the chamber pressure was lowered to ≈2 mTorr before a plasma power of 120 W was applied. As the average etching rate using HCl was ≈100 nm min^{-1}, the etching process was performed in ≈8 min to completely remove the SiC film. We employed a Dektak surface profiler to confirm a negligible overetched thickness of the glass substrate. After the etching process, the photoresist layer was removed (Figure 5, step 7). A 300 nm aluminum layer was deposited using a sputtering process (Figure 5, step 8) and then electrodes were formed via a photolithography process (Figure 5, step 9). Next, the master mould of the cooling channel was designed and fabricated using stereolithography (SLA) technique (da Vinci Nobel 1.0A SLA Resin 3D Printer-XYZprinting, Australia). To this aim, the channel features were printed on the photosensitive resin, washed with ethanol, dried with an air gun, postcured in a UV machine and heated at 80 °C for 24 h. Then, polydimethylsiloxane (PDMS) prepolymer and its curing agent were mixed in a ratio of 10:1 and degassed in a vacuum chamber. Subsequently, the PDMS was poured onto the postcured and postheated master mould and cured for 4 h at 80 °C. It was found that the UV postcuring time and the postheating procedure were critical for realizing the PDMS positive replica from the SLA fabricated master mould.

Finally, the PDMS channel was then bonded to the back of the SiC/glass assisted by oxygen plasma (Figure 5, step 10). Due to the excellent transparency of the SiC film and the glass substrate (Figure 3a), the alignment process to bond PDMS cooling channel to the SiC device was easily performed under a microscope. The

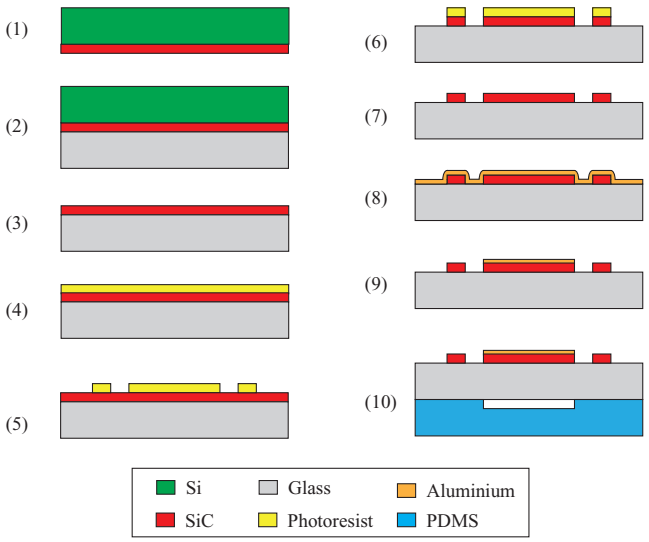

Figure 5. MEMS fabrication process for the SiC cooling device arrays. 1) Growth of SiC nanofilms on Si. 2) Bonding of SiC nanofilms on glass. 3) Formation of SiC/glass platform. 4) Coating of photoresist. 5) Patterning of photoresist. 6) Etching of SiC by Inductively Coupled Plasma. 7) Removing of photoresist. 8) sputtering of aluminum. 9) Etching of aluminum. 10) 3D printing of PDMS channel and oxygen plasma bonding of the PDMS to glass chip.

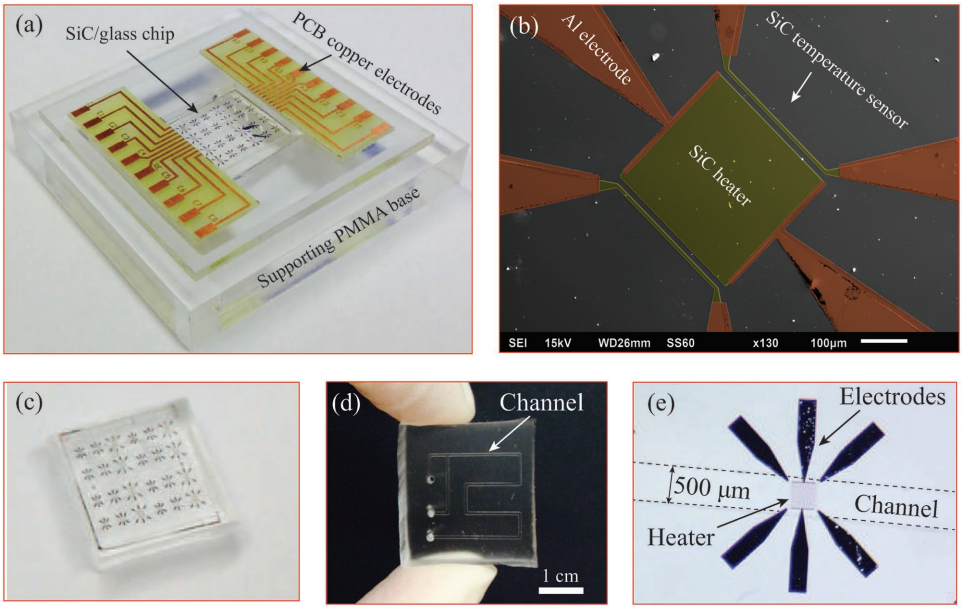

Figure 6. Fabricated device. a) An as-fabricated SiC cooling device with heating/cooling unit arrays, PDMS cooling channel, and engraved supporting PMMA base. b) SEM image of a SiC heating/sensing unit. c) A photograph of the SiC chip aligned on a cooling PDMS channel. d) A photograph illustrating the as-fabricated PDMS channel using a 3D printing technique. e) An optical image of the SiC heater/temperature sensors in align with PDMS cooling channel.

device was then packaged on a PMMA supporting base and PCB electrodes was bonded on the base using glue. **Figure 6**a shows the photo of the as-fabricated SiC device and a zoom-in scanning electron microscopy (SEM) image of the SiC heating/sensing unit is illustrated in Figure 6b. Figure 6c,d shows the SiC device aligned on the PDMS cooling channel and the as-fabricated PDMS channel, respectively. Figure 6e shows an individual SiC heating/sensing unit aligned on a 500 μm wide channel.

2.3. Experimental

The thermoresistive characterization was performed on a hotplate placed in an enclosed chamber with a Resistive Temperature Detector reference temperature sensor (accuracy ±0.1 °C) as shown in the Supporting Information (Figure S5a). An Agilent Source Measure Unit was employed to measure the resistance of the SiC device. The Supporting Information (Figure S5b) shows the schematic sketch of the experimental setup for testing the cooling device. A constant voltage was used to raise the temperature of the heater while the temperature was measured using the integrated SiC temperature sensors around the heater. By measuring the resistance of the temperature sensors, the cooling efficiency of the system was evaluated. In the cooling process, two syringe pumps generated a flow rate of deionized water in a range of 0–3400 μL min^{-1}.

3. Results and Discussions

3.1. Sensing Characteristics of the SiC Device

To confirm the Ohmic contact of the Al electrodes to the SiC nanofilms, we performed current–voltage characterization of the SiC thermoresistors. **Figure 7**a shows the linear *I*–*V* characteristic of the film, indicating the suitability of SiC films as a thermoresistor. Figure 7b shows the dependence of the electrical resistance of SiC thermoresistor on temperature. Evidently, the resistance increases from 684 to 700 Ω when the temperature increases from the room temperature to above 120 °C. The linear relationship between electrical resistance R and temperature T can be expressed as[17,33,34]

$$R = R_o + \alpha(T - T_o) \tag{1}$$

where R_o is the resistance at the reference temperature T_o (25 °C). From the linear fit, a temperature sensitivity of 0.5 Ω K^{-1} was recorded for the highly doped SiC film. To measure the temperature of the SiC chip, the relationship between the chip temperature and the relative resistance change is plotted in Figure 7c. The rate of temperature increase is 43 K per 1% resistance change and the temperature rise on the SiC device can be described as $T = 25\ °C + 43.02 \times \Delta R/R(\%)$. These calibration results will be used to calculate the temperature increase in the SiC device.

3.2. Heating and Cooling Effects

Figure 8a shows the schematic sketch of the device structures with their corresponding thermal resistances. The total thermal resistance R_{total} of the device consists of the glass thermal resistance R_{glass} and the thermal resistance of heat sink to fluid R_{sink}. For an efficient cooling systems, R_{sink} is designed based on the following relationship[35,36]

$$R_{sink} \sim \frac{1}{mC_p\left(1 - e^{-\frac{hA}{mC_p}}\right)} \tag{2}$$

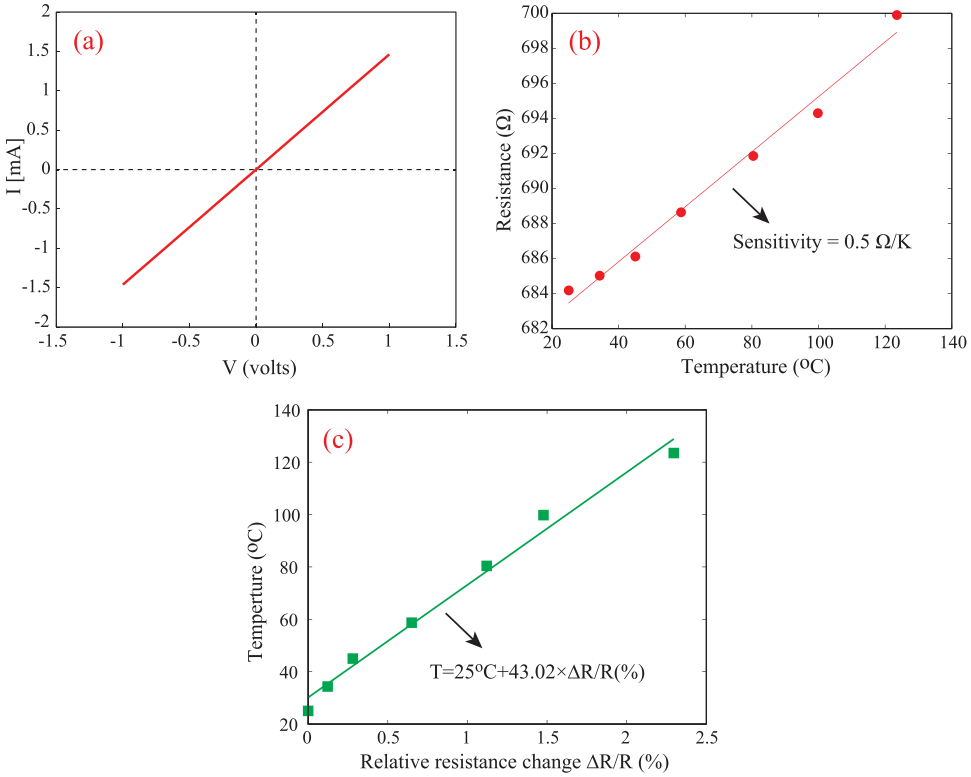

Figure 7. Thermoresistive properties of SiC nanofilms on glass. a) Current–voltage characteristic of SiC thermoresistor. b) The dependence of the electrical resistance of SiC films on temperatures. c) Temperature as a function of the resistance change of SiC nanofilms.

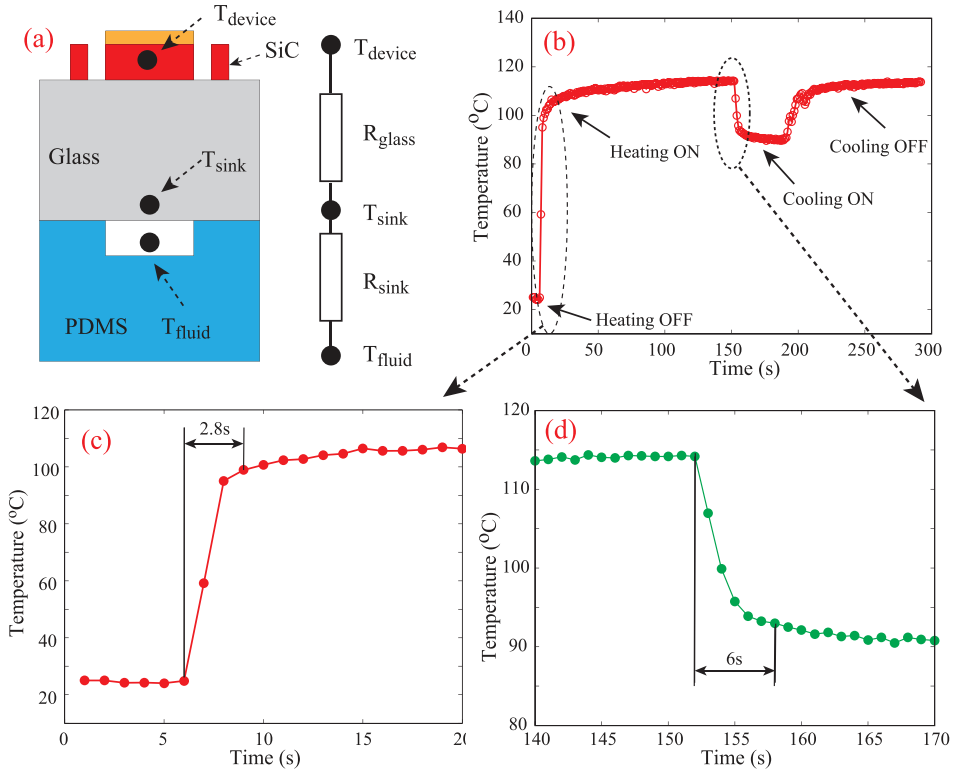

Figure 8. Response of SiC device to heating and cooling. a) Schematic sketch of the device structure with the thermal resistances. b) Temperature change with heating and cooling at an applied voltage of 2.5 V (corresponding to a maximum temperature of 113 °C) and a water flow of 100 µL min^{-1}. c) Time response to the heating is 2.8 s. d) Time response to the cooling is 6 s.

where m and C_p are the mass flow rate (kg s^{-1}) and specific heat capacity (J kg^{-1} K^{-1}) of the fluid, respectively; h is the heat transfer coefficient (W m^{-2} K^{-1}) at the glass-fluid interface; A denotes the effective heat transfer area (m^2). To increase cooling efficiency, the thermal resistance of interface between glass and fluid R_{sink} should be reduced. From Equation (2), the thermal resistance can be improved by increasing the fluid velocity, heat transfer area and heat transfer coefficient. The active cooling efficiency can be directly improved by lowering the thermal resistance of the glass layer. The replacement of Si by glass would increase the thermal resistance by 2 orders of magnitude, while the utilization of nanoscale-thick glass substrate (e.g., Silicon on Insulator (SOI)) would lower the thermal resistance of the glass layer by 5 orders of magnitude. Therefore, future work would be carried out to develop SiC nanofilms on other platforms, such as SOI wafers with a thickness of SiO_2 layers in few nm ranges.

We deployed a single-phase water flow to determine the fluid cooling effect with different applying voltages to the heater. For example, we employed a constant water flow rate of 100 µL min^{-1} to study the cooling effect in the SiC system. Constant DC voltages of 2, 2.5, and 3 V were applied to the SiC heater to initiate the on-chip heating (heating ON, Figure 8b) from the room temperature T_{room} to a temperature T_{max}. Simultaneously, the temperature of the chip was monitored by the resistance of the temperature sensor. We observed that the SiC chip had a temperature of 25 °C (room temperature), which increased to a maximum value of T_{max} = 113 °C when a voltage of 2.5 V was applied. This steady-state temperature was stable until a fluid flow rate of 100 µL min^{-1} was supplied to the cooling channel. The chip temperature dropped by 24 K before returning to its initial steady-state value (113 °C) when the fluid cooling is turned OFF. The cooling effect was observed owing to the heat conduction of glass substrate from the SiC film to the cooling water in the channel.

The thermal response times of heating and cooling were recorded in Figure 8c,d. The 90% thermal response of the SiC nanofilms on glass was measured to be 2.8 s (Figure 8c), corresponding to a bandwidth of 0.357 Hz. After 2.5 min, the cooling system was turned ON by a water flow rate of 100 µL min^{-1} to reduce the device temperature to T_{min}. The chip cooling is defined as $\Delta T = T_{max} - T_{min}$. The cooling rate is then calculated as $C_{rate} = \Delta T/t_c = (T_{max} - T_{min})/t_c$ where t_c = 6 s (Figure 8d) is the response time for the SiC device to change its temperature from T_{max} to T_{min}. When the fluid was turned OFF, the device temperature increased to the initial temperature T_{max}. Figure 8b shows the temperature response of the device with heating ON at 2.5 V, cooling ON with 100 µL min^{-1} and cooling OFF. It is evident that the maximum chip temperature, chip cooling ΔT, and the chip cooling rate are 113±2 °C, 24±1 K, and 0.1 K min^{-1}.

We then conducted the experiments for other heating schemes with maximum temperature of 100–150 °C. Under an applied voltage of 2 V, the SiC chip had an initial steady-state temperature of T_{max} = 100 °C, which dropped by 18 K when the water flow of 100 µL min^{-1} was applied to the cooling channel. At the same fluid flow rate, the cooling temperature increased with increasing device temperatures (**Figure 9**). For example, the cooling temperature ΔT increases from 20 to 35 K at the flow rate of 100 µL min^{-1} when the chip temperature T_{max} increases from 100 to 150 °C. The cooling efficiency at a constant cooling rate is defined as follows

$$\gamma = \frac{\Delta T}{T_{heating}} \tag{3}$$

where $T_{heating} = T_{max} - T_{room}$ is the heating temperature; T_{room} = 25 °C is the room temperature. The cooling efficiency was found in a range of 0.24–0.28 at a constant flow rate of 100 µL min^{-1} when the maximum heating temperatures increased from 100 to 150 °C. **Table 1** shows the performance of the cooling system integrated into the SiC thermal chip.

3.3. Influence of Flow Rate

The experiments were conducted under an applied voltage of 2.5 V to the SiC heater, corresponding to maximum temperature of 113 °C on the SiC chip. The resistance of the SiC temperature sensors was measured under different applied flow rates of DI water (e.g., from 0 to 3400 µL min^{-1}). With the defined configuration of the cooling channel, the Reynolds number was estimated to be less than 167 for the flow rate range of 0–3400 µL min^{-1}, using the following equation[37,38] $R_e = \frac{2V}{\nu(w+h)}$, where V is the water velocity (m^3 s^{-1}), ν is the kinematic viscosity of water (≈10^{-6} m^2 s^{-1} at 20 °C); w = 500 µm and h = 200 µm are the width and height of the PDMS channel. It is evident from **Figure 10** that the absolute value of the average fluid cooling temperature ΔT increases significantly to 20 K when the flow rate increases to 200 µL min^{-1}, equivalent to a cooling rate of 0.1 K(µL min^{-1}). This high efficiency at low flow rates is attributed to the heat transfer to the water flow under the conduction cooling. The temperature rise on the heater will lead to the heat conduction to the PDMS channel through the glass substrate. The water flow absorbs the heat, leading to the increase of the water temperature. The continuous flow results in a higher efficiency of the cooling effect. On the other hand, the cooling rate decreases drastically for the water flow rate from 200 to 500 µL min^{-1} and saturates at a flow rate of above 1000 µL min^{-1}. This is due to the fact that the temperature difference between the glass substrate and the cooling water is close to zero, resulting in the

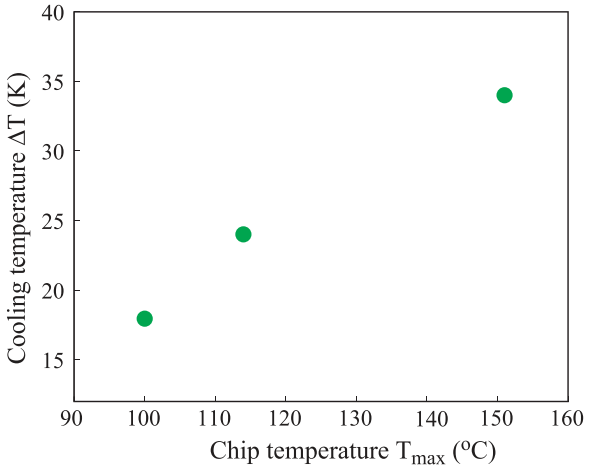

Figure 9. Cooling effect in SiC power device with different heating schemes at a flow rate of 100 µL min^{-1}.

Table 1. Heating and cooling effects in the SiC device compared to the literature.

Voltage	Inte. heating	Inte. sensing	Inte. cooling	Production	T_{max} (°C)	ΔT [K]	Efficiency	Ref.
–	No	No	Yes	Small scale	40	2.9	0.17	[41]
–	No	No	Yes	Small scale	50	4.0	0.15	[41]
–	No	No	Yes	Small scale	50	6.6	0.264	[7]
2 V	Yes	Yes	Yes	Simple, large scale	100	18	0.24	This work
2.5 V	Yes	Yes	Yes	Simple, large scale	113	24	0.273	This work
3 V	Yes	Yes	Yes	Simple, large scale	150	35	0.28	This work

saturation of the sensor response. To overcome this saturation, the heating power of the heater (the temperature of the chip) at higher flow rates must be increased, or a fluid with a higher heat transfer coefficient must be used[39–42] such as two-phase flows.[43] When the density and size of the SiC cells increase, the corresponding density and size of the microfluidic are accordingly adjusted in the computer-aided design process. At a very small size and large density of SiC cells, the hot spots (e.g., heating spots) will be replaced by the relatively uniform temperature distribution on the power chip.[44] Therefore, the alignment of microfluidic channels with the heaters is no longer needed, leading to a simpler design and fabrication of such cooling systems. In addition, the recent fabrication method of free-standing 3C-SiC membranes on 3C-SiC pseudosubstrates would be employed to fabricate microchannels.[45] However, further work should be carried out to liberate long and narrow membranes to function as a microfluidic cooling channel.

4. Conclusion

Our fabrication strategy eliminated the negative impact of the SiC/Si interface and enabled the development of 3C-SiC power electronic devices with integrated heating, sensing, and thermal management systems. The heater and temperature sensors were fabricated from SiC nanofilms grown on Si substrates and transferred to a glass substrate. With an applied voltage of 2–3 V, the maximum temperature of 100–150 °C was raised on the SiC chip. The SiC power device with its cooling system was demonstrated with a high efficiency of 0.28 and a high cooling rate of 0.1 K(μL min^{-1}). This work indicates a potential of using our fabrication method to develop on-chip SiC systems with integrated efficient cooling modules.

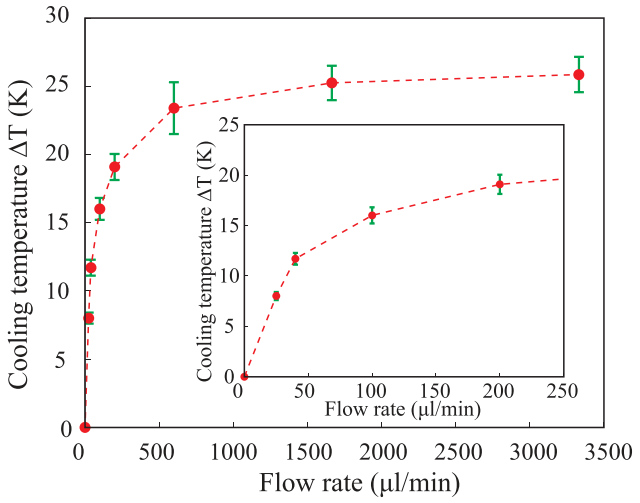

Figure 10. Cooling performance with different flow rates between 0 and 3400 μL min^{-1}. The inset shows the details of the performance at low flow rates (e.g., 0–200 μL min^{-1})

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

microfluidic cooling, power electronics, SiC MEMS, SiC/Si heterostructure, thermoresistive effect

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